**IN THE SPECIFICATION:**

Please insert before the first paragraph under BACKGROUND OF THE INVENTION of page 1 of the disclosure currently on file with the following paragraph:

This application is a Continuation application of U.S. Application No. 10/051,188 filed on January 22, 2002. PAT 6,670,642 Priority is claimed based on U.S. Application No. 10/051,188 filed on January 22, 2002.

Please replace the last paragraph of page 14 (continuing to page 15) of the Disclosure currently on file with the following paragraph:

Referring next to Figure 7B, the vertical Source-Channel-Drain columns (S-C-D) of the [[P]]NMOS transistors Q3, Q4 are formed as follows. A first poly-silicon source layer 38-1 (doped with an n-type impurity, ex. P, As), a first poly-silicon channel layer 40-1 (doped with an p-type impurity, ex. B, $BF_2$), and a first poly-silicon drain layer 39-1 (doped with an n-type impurity, ex. P, As) are deposited in sequence by a CVD method. It is also possible to form the first poly-silicon source layer 38-1, the first poly-silicon channel layer 40-1, and the first poly-silicon drain layer 39-1 by ion-implanting. A first mask layer (completely removed later so it is not shown in the final structure of Figure 7B) is deposited on the surface, then etched away via a first mask to form a pair of first mask caps 41. The first mask caps 41 then are used as a mask for etching into the three poly-silicon layers 38-1, 40-1, 39-1 into two S-C-D columns. A first gate silicon dioxide dielectric layer 36-1 is then deposited all over the surface, including the top and sides of the S-C-D columns.

Please replace the third and fourth paragraphs of page 15 of the Disclosure currently on file with the following paragraphs:

The first mask caps 41 then are again used as a mask for etching back a thin layer from the gate electrode poly-silicon 37-1 and the gate dielectric columns 34-4. And the gate electrode interlayer dielectric 34-4 is again deposited on the whole surface then etched back to [[a]]an even level right above the first mask caps 41. As